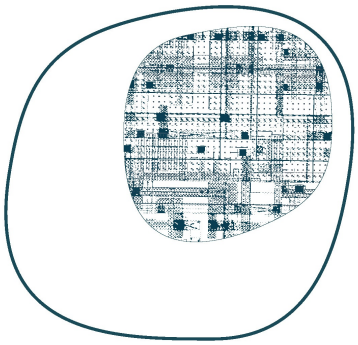

PETsys
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TOFPET2: a high-performance ASIC for time and amplitude measurements of SiPM signals in time-of-flight applications

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ABSTRACT: TOFPET2 is a readout and digitization ASIC featuring low-noise and low-power for time-of flight (TOF) applications using SiPMs. The circuit is designed in standard CMOS 110 nm technology, has 64 independent channels and is optimized for time-of-flight measurement in Positron Emission Tomography (TOF-PET). The input amplifier is a low impedance current conveyor based on a regulated common-gate topology. Each channel has quad-buffered analogue interpolation TDCs (time binning 30 ps) and charge integration ADCs with linear response at full scale (1500 pC). The signal amplitude can also be derived from the measurement of time-over-threshold (ToT). The maximum event rate is 480 kHz per channel, with up to 2 MHz dark counts rejection.

Contents

1. Introduction

Several applications require the measurement of light pulses detected by SiPMs with time resolution in the range $10-100$ ps. Time-of-flight measurements are used in a number of nuclear and particle experiments as well as in PET medical imaging systems that require this performance.
The signal-to-background ratio of PET images can be improved by measuring the Time-of-Flight (TOF) of the two γ photons from positron electron annihilation. The required coincidence time resolution is below 200 ps (FWHM) [1]. Time resolution is strongly limited by the scintillating light yield and transport. For this reason the readout system must be sensitive to the first photo-electrons, as reported in [2]. This leads to the neeed of very high speed and low noise electronics, sensitive to the rising edge of the signal produced by the γ ray detector to obtain the temporal information [3].
Here we present a read out and digitization application-specific-integrate-circuit (ASIC) for TOF-PET applications, based on a regulated common-gate stage, operating as a low noise input current mirror.
The TOFPET2 is a 64-channel mixed-mode ASIC developed in standard CMOS 110 nm technology, which revises and add functionality to a previous chip version [4]. The proposed circuit is optimized for use with SiPMs operating at gain of $1-4\times10^6$. The circuit provides also linear amplitude measurement in the full dynamic range of input pulse charge (1500 pC). The maximum input charge corresponds to 2500 p.e. detected by devices with gain 3.5×10^6.

2. ASIC Architecture

The TOFPET2 ASIC general architecture is based on the previous chip version [4] but has significant differences. In particular, the new chip includes pulse amplitude measurement based on charge integration and allows significant higher input and output data rates. The new requirements implied the redesign of the frontend amplifiers, the addition of a charge integrator and the full redesign of the digital logic.

The ASIC provides time and energy digitization of signals from 64 photo-sensor channels. While the circuit can operate with different photo-sensors, its performance was optimized for SiPMs. The ASIC has two selectable preamplifiers per channel allowing operation either with positive or negative polarity signals.

The readout scheme of one channel is depicted in figure 1. The selected preamplifier provides a signal to two post-amplifiers and a pulse-charge integrator. The post-amplifiers, separately specialized for time resolution and pulse triggering, have an adjustable transimpedance gain and provide voltage signals to two discriminators.

One discriminator is used for timing measurement with a programmable threshold down to a few photo-electrons. A second discriminator has higher threshold and is used for on chip rejection of low amplitude signals.

The signals from the discriminators are fed to a digital logic block, working at 200 MHz clock frequency, that controls two time-to-digital converters (TDC) and a charge integrator.

The first TDC measures the phase of the rising edge of the low threshold discriminator output with respect to the reference clock, while the second TDC measures the falling edge of the high threshold discriminator output. The mixed mode TDC block is based on four-fold time-to-analogue converter (TAC), for signal de-randomization and a 10 bit Wilkinson analogue-to-digital converter (ADC). The TDC has 30 ps time binning.

The channel digital logic controls also the charge integration time interval, which can be configured with different options. The output of the charge integrator is digitized by a Wilkinson ADC. One out of two ADCs per channel is configured to measure either the charge amplitude (default mode) or the fine time of the falling edge of the high threshold discriminator. In the former case, the sec-

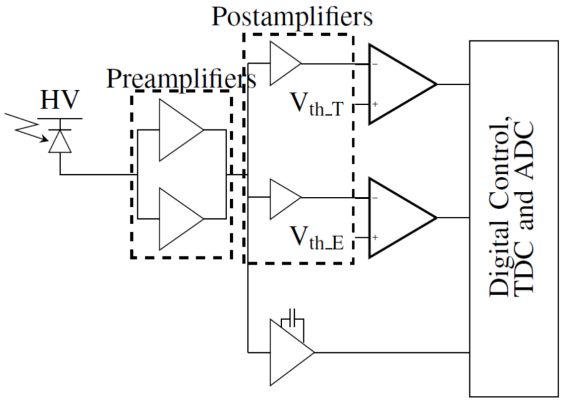

Figure 1. Top level scheme of the single channel.

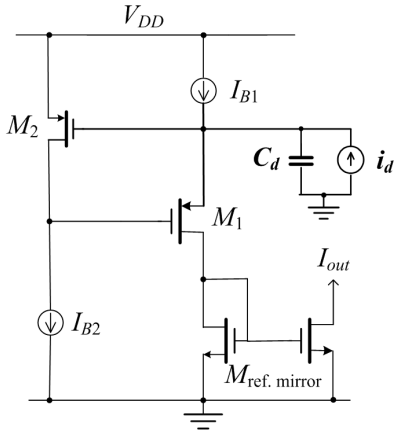

Figure 2. Simplified preamplifier circuit.

ond time measurement has the resolution of the coarse time counter (200 MHz clock period). The time difference of the two measurements can be used to compute the time-over-threshold (ToT) which is dependent on the pulse amplitude. The digital data corresponding to each input pulse (event) is stored in local buffers waiting to be transferred to the global output FIFO. Each event is identified by the coarse time tag (clock counter) and by the channel identifier. The output data is transmitted by 1 to 4 LVDS links working up to 640 Mbit/s each.

3. Frontend Amplifiers and Discriminators

The preamplifiers are two selectable current conveyors, for positive and negative polarity signals, based on a modified version of the regulated common-gate transimpedance amplifier (TIA) [6]. The conveyors provide a low input impedance for the detector and a high impedance current output. The circuit for the positive signal version is showed in figure 2. It is an upgraded version of the preamplifier already proposed in [4], redesigned and optimized to extend the dynamic range while preserving the timing performance. The negative signal version has the same topology, with the transistors, either NMOS or PMOS, switched to the complementary type. A pre-amplifier provides a low-frequency amplification of 25 dB and pass-band of 330 MHz and has power consumption of 2.5 mW.

The post-processing is done by two transimpedance amplifiers and an integrator. The preamplifier is connected to the TIAs in AC mode. Each TIA is a PMOS current mirror replicating the AC part of the preamplifier current output on a 3 kΩ resistor.

The two TIAs feed discriminators. The first discriminator uses a configurable low threshold at the level of 1 to 20 p.e., with resolution selectable between 0.5 and 0.1 p.e. The other discriminator has configurable threshold up to 1000 p.e. for on chip event selection.

4. Charge Integrator

The charge integrator processes the output signal of the preamplifier within a time window that

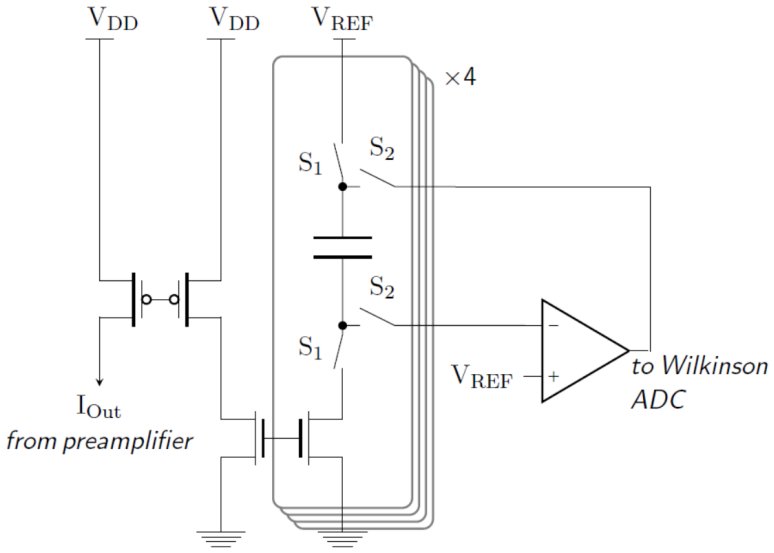

Figure 3. Simplified integrator scheme.

is generated by the digital logic, based on the discriminators output. In this scheme, four flipped capacitors sharing a single readout differential amplifier perform the signal integration, allowing de-randomization of the signals. The analogue signals are fed to a 10-bit analogue-to-digital converter (ADC) ADC for conversion. A simplified version of the integrator is depicted in figure 3. The range of the integrator, specified in p.e. for a SiPM gain of 1.25×10^6, can be selected among a set of possible ranges: $7.5 - 750$ p.e., $15 - 1500$ p.e., $30 - 3000$ p.e. and $60 - 6000$ p.e. These different ranges allow the use of the integrator in different schemes of PET crystals read-out, namely 1:1 coupling of crystal pixels to SiPM pixels and light sharing schemes, in which the light generated in a LYSO crystal is readout by several SiPMs pixels.

5. TDC/ADC and Digital Control

The TDC/ADCs are controlled by the digital block following the strategy described below. The signal at the output of the timing branch discriminator is a pulse-width-modulated binary signal (PWM), referred as DOT. The rising edge of the DOT signal, triggers another PWM signal, the W_TAC_T signal. The rising edge of W_TAC_T corresponds to the rising edge of DOT, and its falling edge corresponds to the second rising edge, after triggering, of the 200 MHz clock signal distributed to the TDC. This ensures a duration of the pulse of at least one clock period, preventing very narrow signals that could be produced if the triggering edge of the DOT and the rising edge of the clock were very close.

The W_TAC_T signal drives a constant current source. This current source discharges a capacitor, called TAC_cap (for time to analog converter capacitor), previously charged to a known value. The voltage across the TAC_cap depends linearly on the time duration of the W_TAC_T signal. After the TAC has converted a time information to an analog voltage, this voltage is digitized by the Wilkinson ADC. The working principle of the digitization is described below.

An active system discharges a second pre-charged capacitor, whose capacitance is 4 times the capacitance of the TAC_cap, called 4X_TAC_cap. The 4X_TAC_cap is recharged by a second constant current source 32 times weaker than the current source discharging the TAC_cap. The recharging time is proportional to the W_TAC_T signal duration, with a multiplication factor of 128, given by the factor 4 for the discharged capacitance and the factor 32 for the recharging current. The difference between the values of a clock counter at the beginning and at the end of the recharging period will give the time duration of the recharge with the resolution of a clock period.

6. Back-End Readout

The 64 channels data readout is handled by a global controller using an external clock up to 320 MHz, that builds-up the event data and runs the interface with the data acquisition back-end. The data above the trigger threshold are sent out in push mode. Each event consists of an event time tag, a channel identifier, and the time and amplitude measurements. Data transmission uses 64/66bit encoding to allow clock recovery and alignment of the data stream at the receiver. The ASIC has 4 output LVDS links working at up to 640 Mbit/s. The performance in terms of output rate capability allows up to 480 kHz average event rate per channel, and a dark counts rejection up to 2 MHz with negligible dead time. The possible settings are resumed in table 1.

Ext. Clock(MHz)	Bin Width (ps)	Data Rate (Mbit/s)	Event Rate/channel (kHz)
160	50	320	240
200	40	400	300
320	50	640	480
400[1]	40[1]	800[1]	600[1]

[1] Available for a future version.

Table 1. Clock, resolution and data rate settings available, and relative maximum event rate per channel.

7. Conclusions

The presented ASIC was designed to achieve a time resolution better than 100 ps for 1 p.e. signals generated by a SiPM, together with a linear amplitude response up to 3000 p.e. distributed in time according to the characteristic LYSO crystal light decay time. The design provides a wide range of configuration options, allowing for example to operate the ASIC in different PET light collection schemes like one-to-one coupling of LYSO crystals to SiPM pixels or light-sharing among several SiPM pixels. Additionally two different methods of pulse amplitude measurement are available, namely charge integration or ToT. The chip can operate with negligible dead time up to 480 kHz event rate per input channel, fulfilling the needs of all current or foreseen PET applications. The specified performances are achieved within the limited power budget of 5 mW per channel, in the case of SiPMs gain of 1.25×10^6.

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